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Wide-Band Current Starved Ring CMOS Voltage Controlled Oscillator (VCO) using 0.18 µm CMOS Technology

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Abstract

This paper describes a design and implementation of Current Starved CMOS Voltage Controlled Oscillator based on Ring Oscillator. Efforts are made to design a CMOS Voltage controlled oscillator having wide frequency range with High frequency, Low power. So, the CMOS VCO designed here having a Five Stage Current Starved CMOS VCO and Seven Stage Current Starved CMOS VCO. The design is optimization and simulates on TSMC 180nm CMOS process at 1.8 V supply voltages. The Five Stage CS VCO results show that the oscillation frequency of VCO varies between 18.724MHz to 1890.4MHz and power consumption may varies between 35.39 µW to 25.013 µW and the Seven stage CS VCO results show that the oscillation frequency of VCO varies between 68.971MHz to 2099.5 MHz and power consumption may varies between 2.59 µW to 348.81 µW.

Keywords: Mentor Graphics; voltage controlled oscillator; ring oscillator; source coupled oscillator.

Introduction

A CMOS Voltage controlled oscillator (VCO) is a critical building block in PLL which decides the power consumed by the PLL and area occupied by the PLL. VCO constitute a critical component in many RF transceivers and are commonly associated with signal processing tasks like frequency selection and signal generation. RF transceivers of today require programmable carrier frequencies and rely on phase locked loops (PLL) to accomplish the same. These PLLs embed a less accurate RF oscillator in a feedback loop, whose frequency can be controlled with a control signal. Transceivers for wireless communication system contain low-noise amplifiers, power amplifiers, mixers, digital signal-processing chips, filters, and phase-locked loops.

Voltage controlled oscillators play a critical role in communication systems, providing periodic signals required for timing in digital circuits and frequency translation in radio frequency Circuits. Their output frequency is a function of a control input usually a voltage. An ideal voltage-controlled voltage oscillator is a circuit whose output frequency is a linear function of its control voltage. Most application required that oscillator be tunable, i.e. their output frequency be a function of a control input, usually a voltage.

There are two different types of voltage controlled oscillators used in PLL, Current starved VCO and Source coupled VCO .In recent years LC tank oscillators have shown good phase-noise performance with low power consumption. However, there are some disadvantages. First, the tuning range of an *LC*-oscillator (around 10 - 20%) is relatively low when compared to ring oscillators (>50%). So the output frequency may fall out of the desired range in the presence of process variation. Second, the phase-noise performance of the oscillators highly depends on the quality factor of on-chip spiral inductors. For most digital CMOS processes, it is difficult to obtain a quality factor of the inductor larger than three. Therefore, some extra processing steps may be required. Finally, on-chip spiral inductors occupy a lot of chip area, typically around 200 *200-300 * 300 m^2, which is undesirable for cost and yield consideration.

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The ring oscillators, however, do not have the complication of the on-chip inductors required for the LC oscillators. Thus the chip area is reduced. In addition to a wide tuning range; ring oscillators with even number of delay cells can produce quadrature-phase outputs. The phase noise performance of ring oscillators is much poorer in general. Also, at high oscillation frequencies, the power consumption of the ring oscillators may not be low which is a key requirement for battery operated devices. To overcome these problems, we work on five and Seven stages current starved Oscillator. Finally their performances are compared based on their results.

Circuit Description

A. Current Starved VCO

The current-starved VCO is shown schematically in Figure. [1]. Its operation is similar to the ring oscillator discussed as above. MOSFETs M2 and M3 operate as an inverter, while MOSFETs Ml and M4 operate as current sources. The current sources, Ml and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for current. The MOSFETs M5 and M6 drain currents are the same and are set by the input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage. An important property of the VCO used in any of the CMOS DPLLs discussed here is the input impedance.

The filter configurations we have discussed rely on the fact that the input resistance of the VCO is practically infinite and the input capacitance is small compared to the capacitances present in the loop filter. Attaining infinite input resistance is usually an easy part of the design. For the charge-pump configuration, the input capacitance of the VCO can be added to C2.

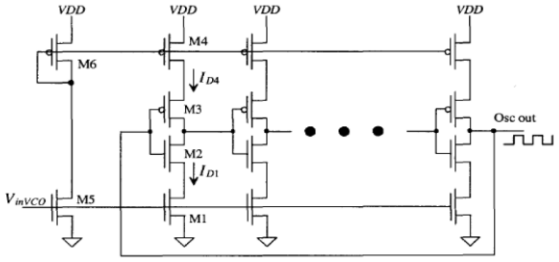

Figure 1. Current-starved VCO[1],[2],[7],[12]

B. Five and Seven stage Current Starved CMOS VCO.

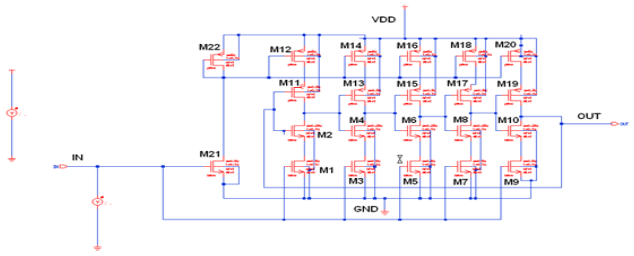

Figure 2. Five Stage Current Starved CMOS Voltage Controlled Oscillator in IC Schematic Editor

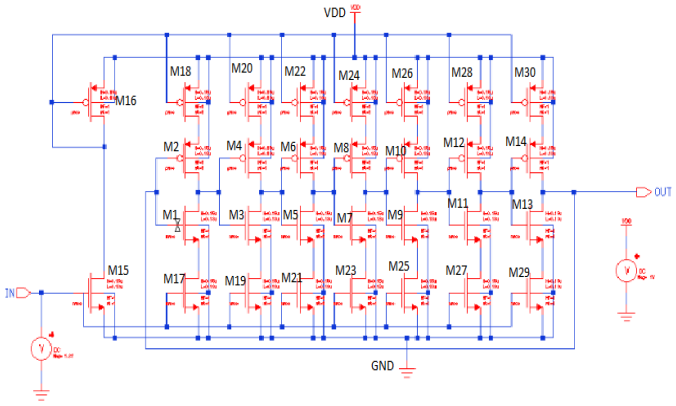

Figure 3. Seven Stage Current Starved CMOS Voltage Controlled Oscillator in IC Schematic Editor

To determine the design equations for use with the current-starved VCO, consider the simplified schematic of one stage of the VCO as shown in Figure [1]. The total capacitance on the drains of M2 and M3 is given by,.

$$C_{tot} = \overbrace{C_{out} + C_{in}C_{in'}(W_pW_p + W_nW_n)}^{\text{Cout}} + \overbrace{\frac{3}{2}C_{ox'}(W_pW_p + W_nW_n)}^{\text{Cin}} \quad (1.1)$$

This equation can be written in a more useful form as,

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$$C_{tot} = \frac{5}{2} C_{ox'} \left(W_p W_p + W_n W_p \right) \quad (1.2)$$

The time it takes to charge *Ctot* from zero to *VSP* with the constant-current *ID4* is given by

$$t1 = Ctot \frac{V_{SP}}{I_{D4}} \quad (1.3)$$

While the time it takes to discharge *Ctot* from VDD to V*SP* is given by,

$$t_2 = C_{tot} \frac{V_{DD} - V_{SP}}{I_{D1}} \quad (1.4)$$

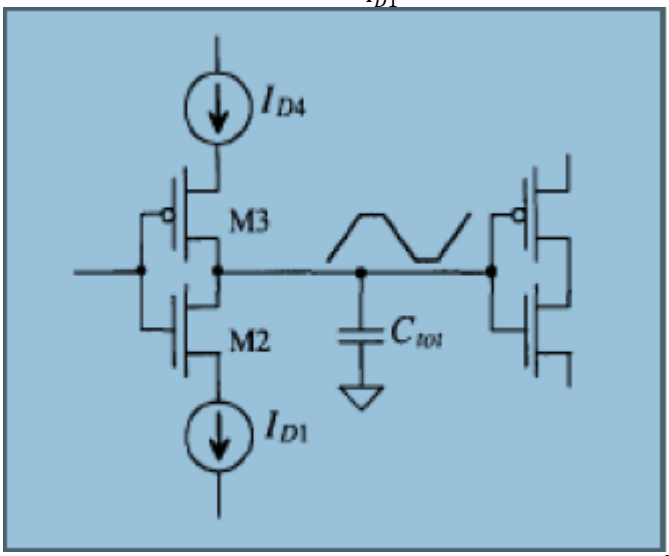

Figure 4. Simplified view of a single stage of the current-starved VCO[1],[12]

If we set ID4 = *ID1* = *ID* (which we will label IDcenter when Vinvco =VDD/2), then the sum of t1 and t2 is simply,

$$t_1 + t_2 = C_{tot} \frac{V_{DD}}{I_D} \quad (1.5)$$

The oscillation frequency of the current-starved VCO for N (an odd number ≥5) of stages is,

$$F_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{N C_{tot} V_{DD}} \quad (1.6)$$

which is equal to

$$= f_{center} \left(@V_{inVco} = \frac{V_{DD}}{2} \; and \; I_D + I_{Center} \right) \quad (1.7)$$

Equation (1.7) gives the center frequency of the VCO when *ID* = *IDcenter*. The VCO stops oscillating, neglecting sub threshold currents, when *Vinvco* < *VTHN*. Therefore we can define,

$$V_{min} = V_{THN} \; and \; f_{min} = 0 \quad (1.8)$$

The maximum VCO oscillation frequency, *fmax* , is determined by finding *ID* when *VinVCO* = VDD. At the maximum frequency then, V*max* =VDD.

The output of the current-starved VCO shown in Figure [2] normally has its output buffered through one or two inverters. Attaching a large load capacitance on the output of the VCO can significantly affect the oscillation frequency or lower the gain of the oscillator enough to kill oscillations altogether.

The average current drawn by the VCO is

$$I_{avg} = N \frac{V_{DD} \cdot C_{tot}}{T} = N \cdot V_{DD} \cdot C_{tot} \cdot F_{osc} \quad (1.9)$$

Or $$I_{avg} = I_D \quad (1.10)$$

The average power dissipated by the VCO is,

$$P_{avg} = V_{DD} \cdot I_{avg} = V_{DD} \cdot I_D \quad (1.11)$$

If we include the power dissipated by the mirror MOSFETs, M5 and M6, the power is doubled from that given by Eq. (1.11), assuming that *ID = ID5 = ID6* . For low-power dissipation we must keep *ID* low, which is equivalent to stating that for low-power dissipation we must use a low-oscillation frequency.

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Simulation Results

A. Five Stage Current Starved CMOS VCO

Fig 2.shows the output waveforms of five stage current starved VCO. Thus it is noted that at a constant control voltage of 1.8V the output frequency of current starved VCO is 1890.4 MHz Simulation results reported that the power consumption is 25.013µW @ 1.8 VDD.

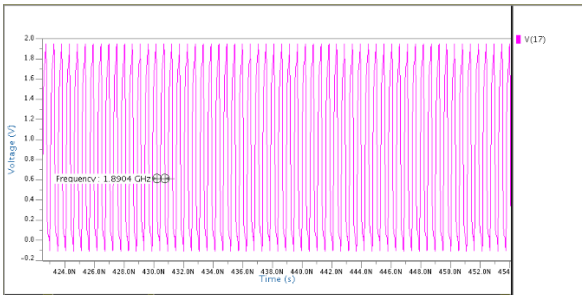

Figure 5. Output Waveform for 1.8v control voltage of Five Stage Current Starved VCO in 180nm Technology.

When the control voltage is varied from 0.5V to 1.8V, the. Oscillation frequency of the designed current starved VCO ranges from 18.724 MHz to 1890.4 MHz Table I. gives the characteristics of the current starved VCO i.e. control voltage (V) Vs frequency (MHz).

Table 6.5 Simulated Results for Five Stage Current Starved CMOS VCO in 180nm Technology

Control Voltage (V)	Reference	Oscillating Frequency (MHz)	Power Dissipation (W)
0.5	129.03	18.724	3.5398E-05
0.6	147.05	112.12	2.0212E-04
0.7	167.29	349.95	5.7016E-04
0.8	178.57	641.17	9.0400E-04
0.9	188.67	924.86	1.1475E-03
1.0	192.30	1024.22	1.1475E-03
1.1	198.01	1366.3	1.5373E-03
1.2	203.99	1513.6	1.7109E-03
1.3	208.62	1631.1	1.8755E-03
1.4	212.24	1714.7	2.3313E-03
1.5	212.77	1773.5	2.1763E-03
1.6	216.00	1825.6	2.3060E-03
1.7	216.37	1862.6	2.4148E-03
1.8	222.53	1890.4	2.5013E-03

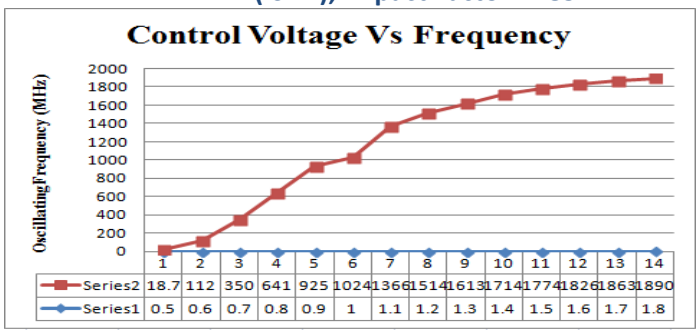

Figure 6. Control Voltage versus Output Frequency Plot for Five Stage Current Starved VCO in 180nm Technology.

B. Seven Stage Current Starved CMOS VCO

Fig 3.shows the output waveforms of seven stage current starved VCO. Thus it is noted that at a constant control voltage of 1.8V the output frequency of current starved VCO is 2.0995 GHz Simulation results reported that the power consumption is 348.81µW @ 1.8 VDD.

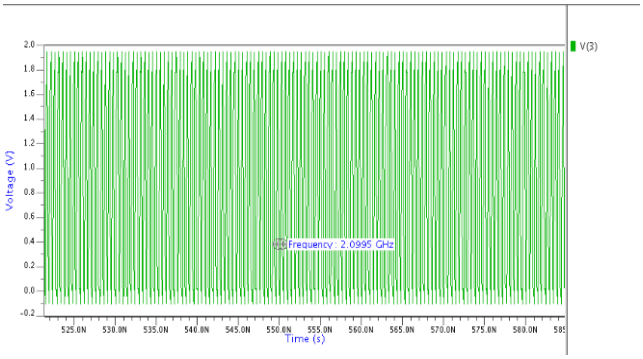

Figure 7. Output Waveform for 1.8v control voltage of Seven Stage Current Starved VCO in 180nm Technology.

When the control voltage is varied from 0.5V to 1.8V, the Oscillation frequency of the designed current starved VCO ranges from 10.020 MHz to 2099.5 MHz Table I. gives the characteristics of the current starved VCO i.e. control voltage (V) Vs frequency (MHz).

Table 6.5 Simulated Results for Seven Stage Current Starved CMOS VCO in 180nm Technology

Control Voltage (V)	Oscillating Frequency (MHz)	Power Dissipation (W)
0.5	68.971	1.7543E-05
0.6	265.30	6.7827E-05
0.7	583.85	1.3435E-04
0.8	926.43	1.7921E-04
0.9	1240.8	2.1489E-04

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1.0	1480.0	2.4610E-04
1.1	1666.5	2.7374E-04
1.2	1797.1	2.9603E-04
1.3	1888.3	3.1178E-04
1.4	1953.5	3.2314E-04
1.5	1997.5	3.3178E-04
1.6	2037.0	3.3868E-04
1.7	2073.3	3.4419E-04
1.8	2099.5	3.4881E-04

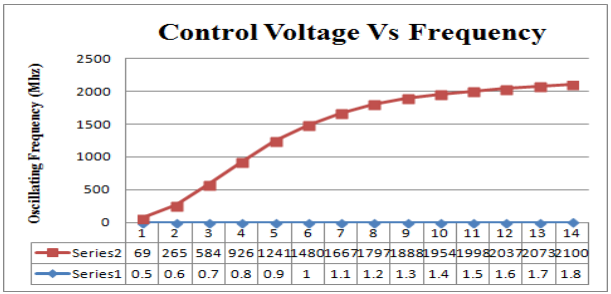

Figure 8. Control Voltage versus Output Frequency Plot for Seven Stage Current Starved VCO in 180nm Technology.

Summary of Results

Parameters	Reference	5-Stage CS VCO	7-Stage CS VCO
Technology	0.18µm	0.18µm	0.18µm
Supply Voltage (V)	1.8	1.8	1.8
I/P Tuning Range(V)	0.1 to 1.8	0.5 to 1.8	0.5 to 1.8
Range of Oscillating Frequency (MHz)	129.03 to 222.53	18.724 to 1890.4	68.971 to 2099.5
Power Consumption (µW)	58.47µW	35.39 to 25.013	2.59 to 348.81
Gate Length	0.18µm	0.18µm	0.18µm

Conclusion

In this paper shows the single stage source coupled CMOS voltage controlled oscillator simulated in ELDO SPICE simulator having high oscillation frequency and low power dissipation. The oscillator can be used for low-voltage low-power application.

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